



US009412868B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.:** **US 9,412,868 B2**
(45) **Date of Patent:** **Aug. 9, 2016**

(54) **SEMICONDUCTOR DEVICE AND
FABRICATION METHOD THEREOF**

(71) Applicant: **TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY,
LTD.**, Hsinchu (TW)

(72) Inventors: **Yen-Ru Lee**, Hsinchu (TW); **Ming-Hua
Yu**, Hsinchu (TW); **Tze-Liang Lee**,
Hsinchu (TW); **Chii-Horng Li**, Jhu-Bei
(TW); **Pang-Yen Tsai**, Jhu-Bei (TW);
Lilly Su, Chu-Bei (TW); **Yi-Hung Lin**,
Taipei (TW); **Yu-Hung Cheng**, Hsinchu
(TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR
MANUFACTURING COMPANY,
LTD.** (TW)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/475,107**

(22) Filed: **Sep. 2, 2014**

(65) **Prior Publication Data**

US 2014/0367768 A1 Dec. 18, 2014

Related U.S. Application Data

(62) Division of application No. 13/248,319, filed on Sep.
29, 2011, now Pat. No. 8,835,267.

(51) **Int. Cl.**

H01L 29/76 (2006.01)
H01L 29/78 (2006.01)
H01L 21/8234 (2006.01)
H01L 21/8238 (2006.01)
H01L 21/306 (2006.01)
H01L 29/04 (2006.01)
H01L 29/06 (2006.01)

H01L 29/08 (2006.01)

H01L 29/66 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 29/7848** (2013.01); **H01L 21/30604**
(2013.01); **H01L 21/823412** (2013.01); **H01L**
21/823418 (2013.01); **H01L 21/823425**
(2013.01); **H01L 21/823481** (2013.01); **H01L**
21/823807 (2013.01); **H01L 21/823814**
(2013.01); **H01L 21/823878** (2013.01); **H01L**
29/045 (2013.01); **H01L 29/0653** (2013.01);
H01L 29/0847 (2013.01); **H01L 29/66636**
(2013.01); **H01L 29/7845** (2013.01); **H01L**
29/66545 (2013.01)

(58) **Field of Classification Search**

USPC 257/190, 255, 286, 288, 327, 348, 369,
257/410; 438/131, 149, 154, 197, 198

See application file for complete search history.

(56)

References Cited

U.S. PATENT DOCUMENTS

6,087,235 A * 7/2000 Yu 438/300
2008/0237634 A1 10/2008 Dyer et al.

(Continued)

Primary Examiner — Errol Fernandes

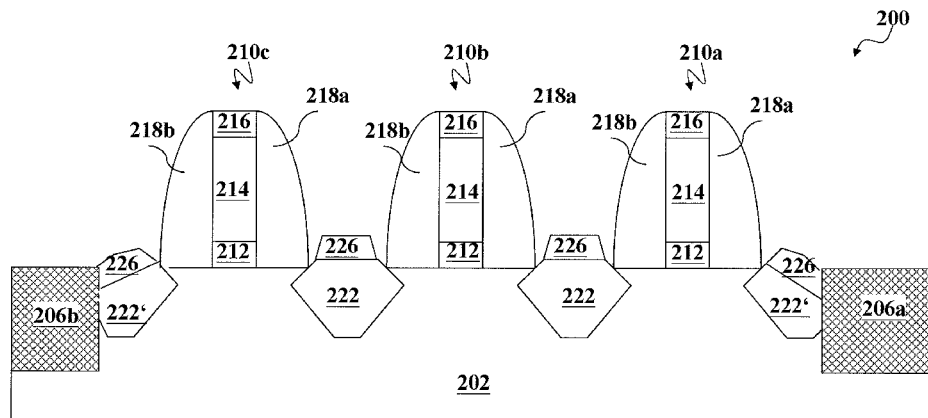
(74) Attorney, Agent, or Firm — Hauptman Ham, LLP

(57)

ABSTRACT

A method for fabricating a semiconductor device includes forming an isolation feature in a substrate, forming a gate stack over the substrate, forming a source/drain (S/D) recess cavity in the substrate, where the S/D recess cavity is positioned between the gate stack and the isolation feature. The method further includes forming an epitaxial (epi) material in the S/D recess cavity, where the epi material has an upper surface which including a first crystal plane. Additionally, the method includes performing a redistribution process to the epi material in the S/D recess cavity using a chlorine-containing gas, where the first crystal plane is transformed to a second crystal plane after the redistribution.

20 Claims, 10 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

2010/0093147 A1 4/2010 Liao et al.

2010/0136761 A1

6/2010 Han

2011/0117732 A1

5/2011 Bauer et al.

* cited by examiner

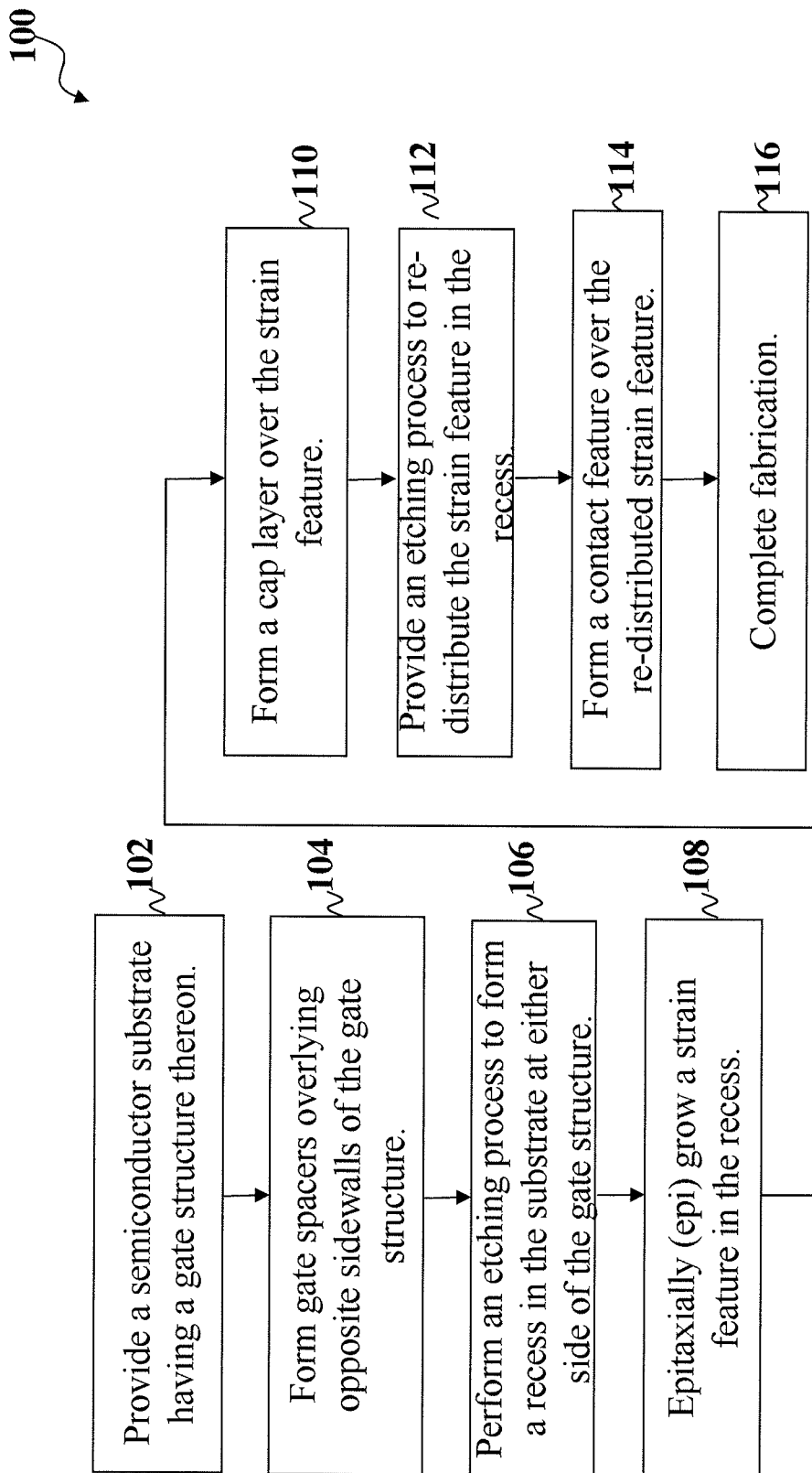


Fig. 1

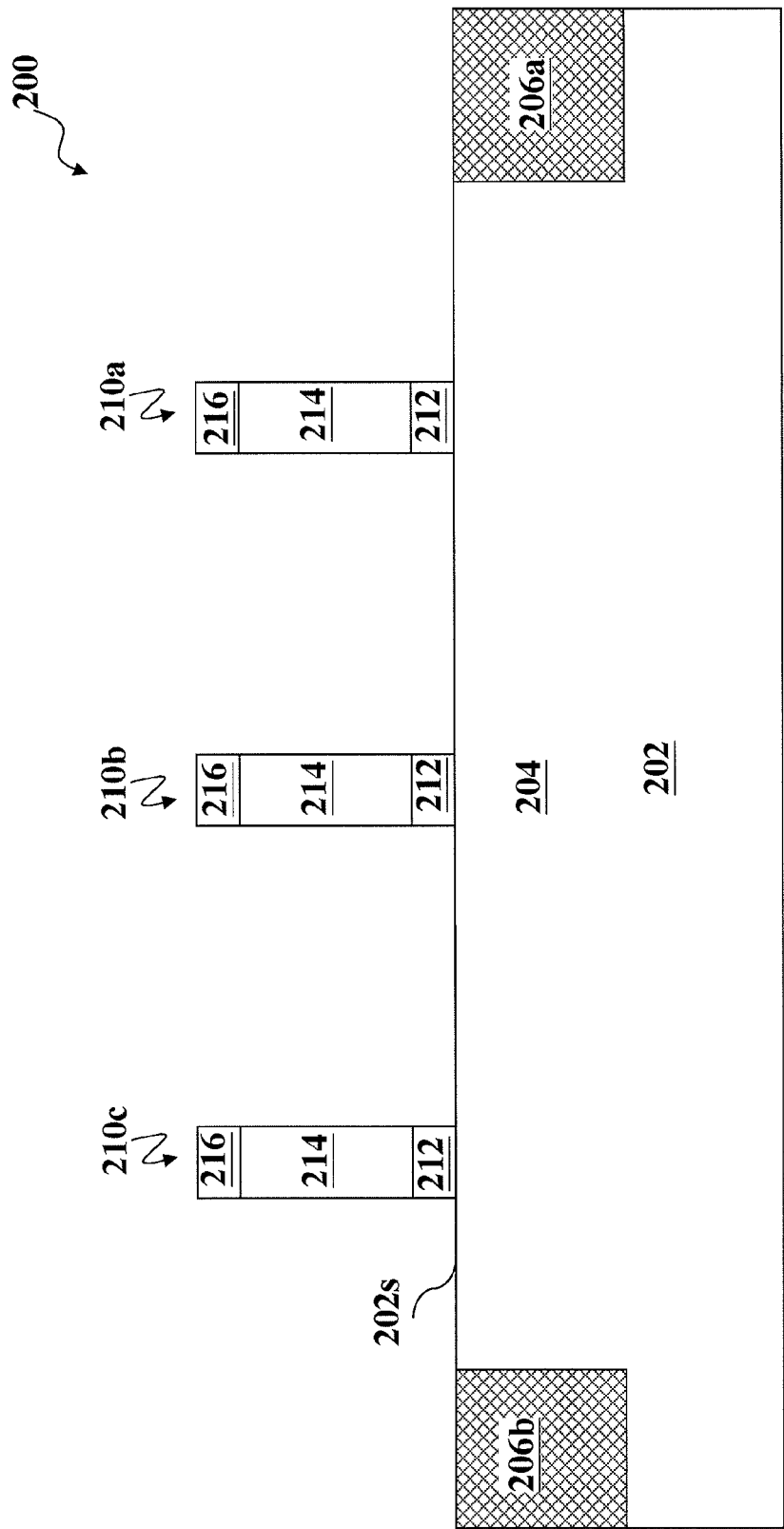


Fig. 2

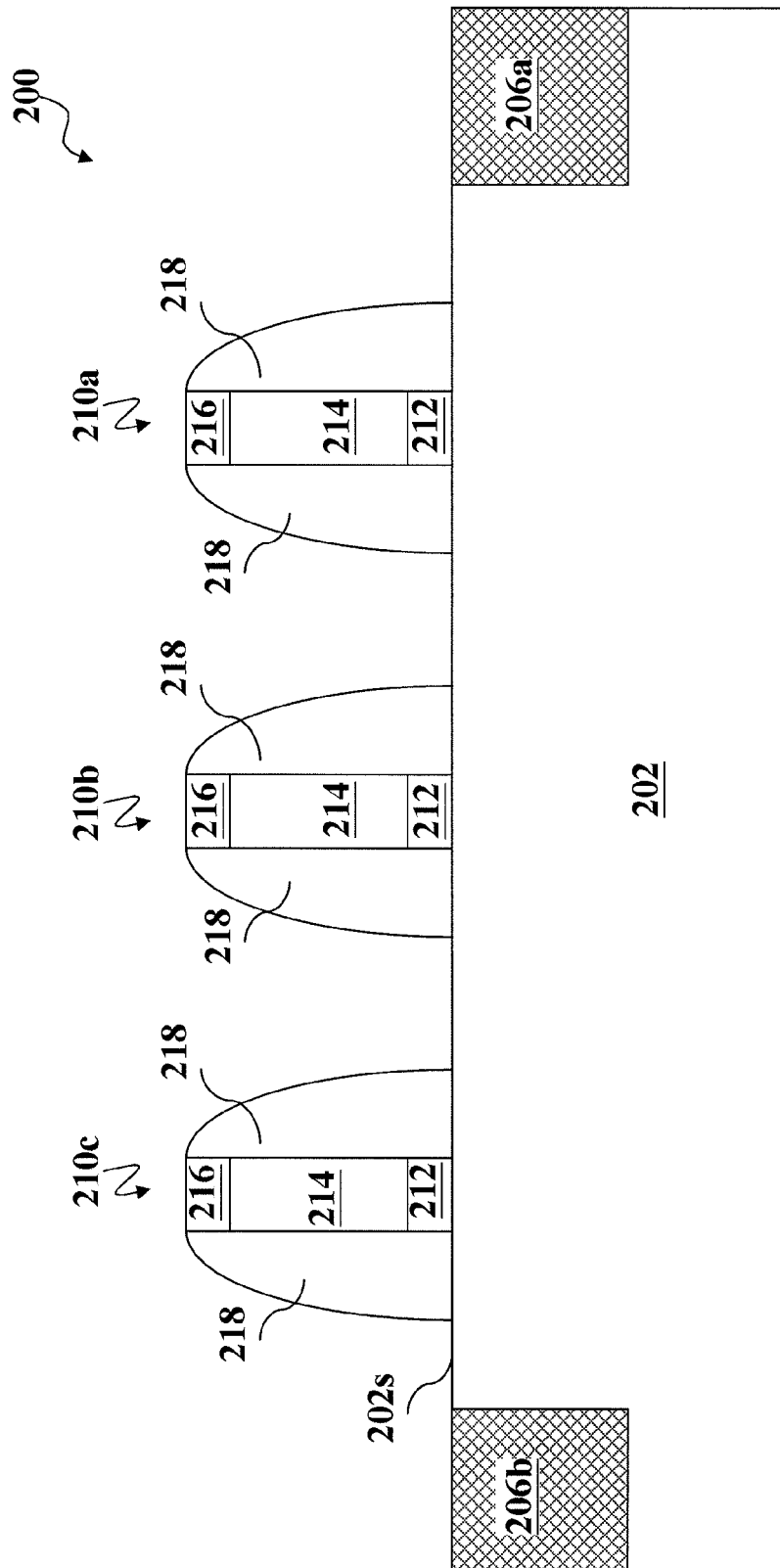


Fig. 3

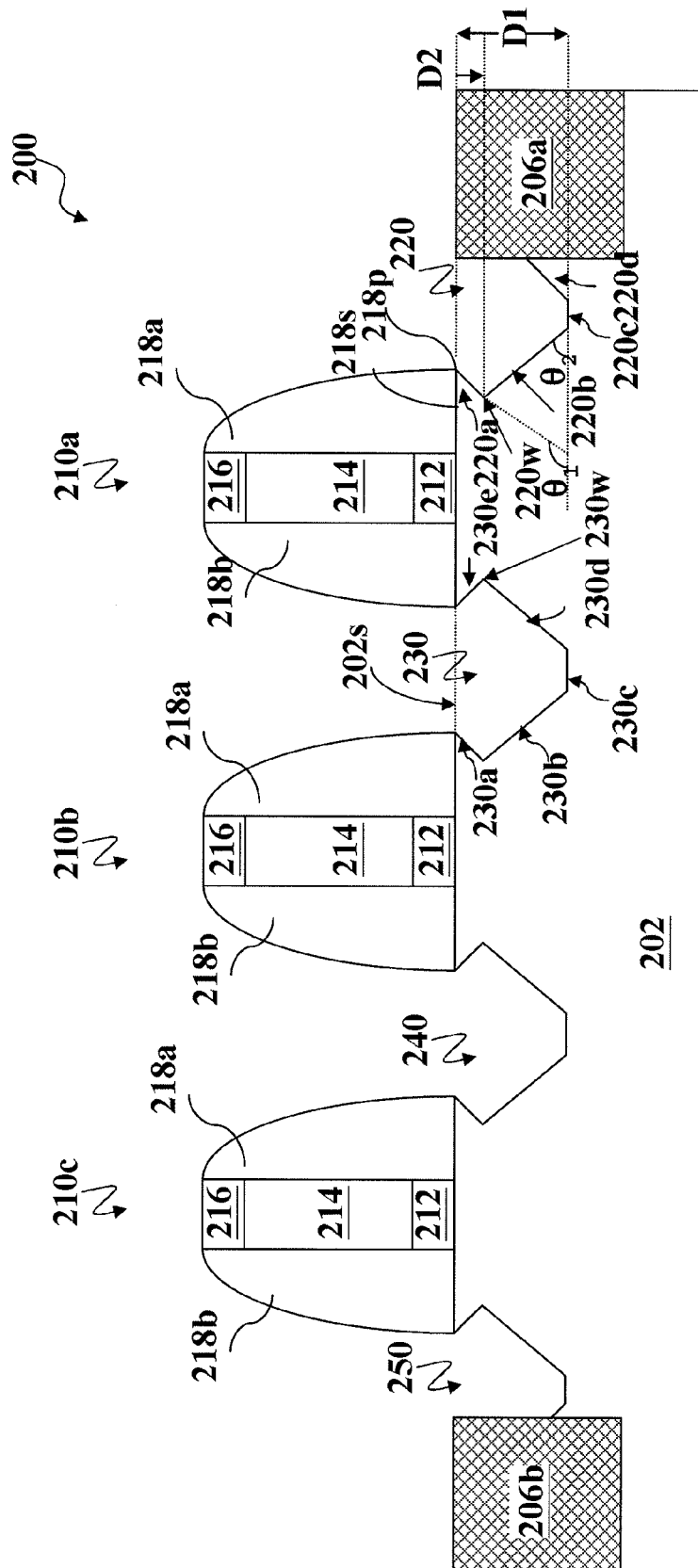


Fig. 4

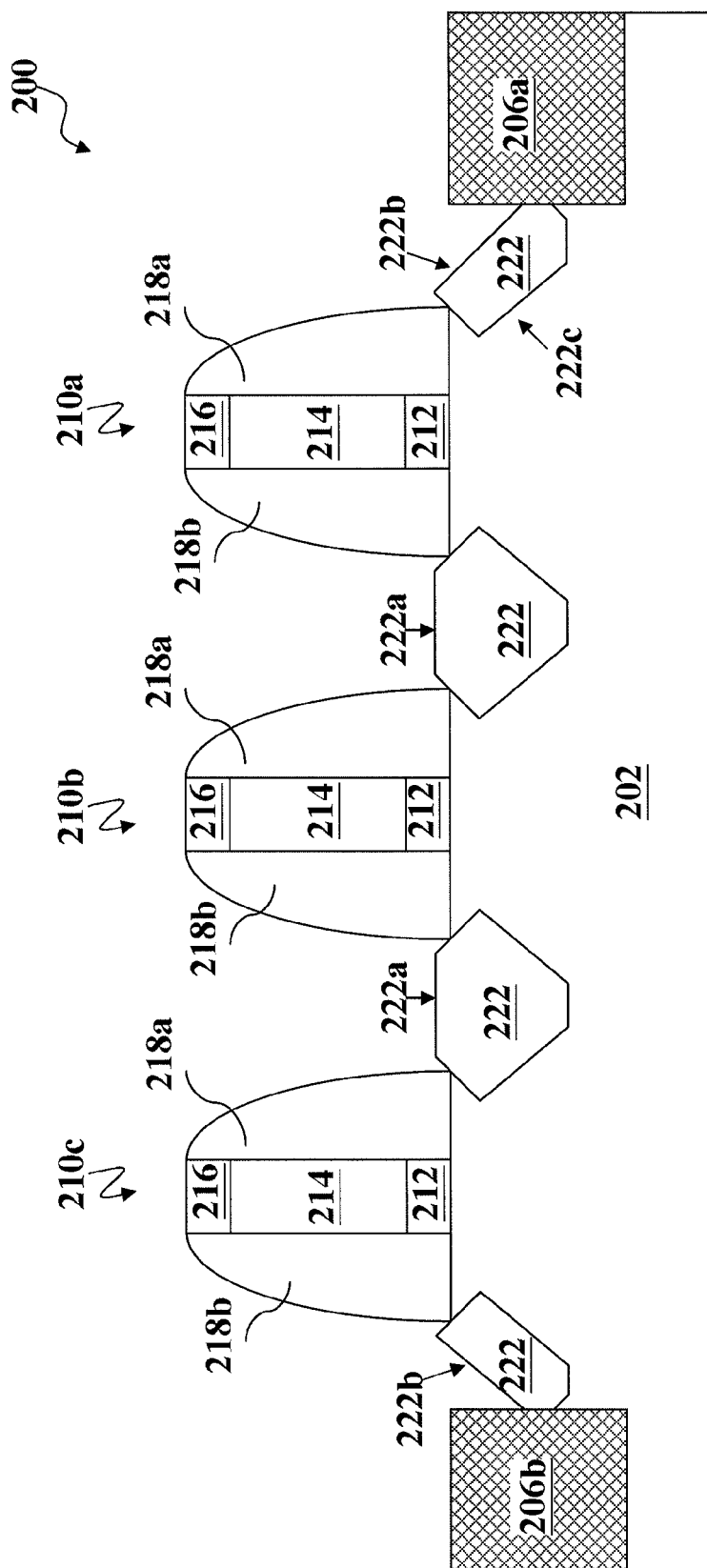


Fig. 5

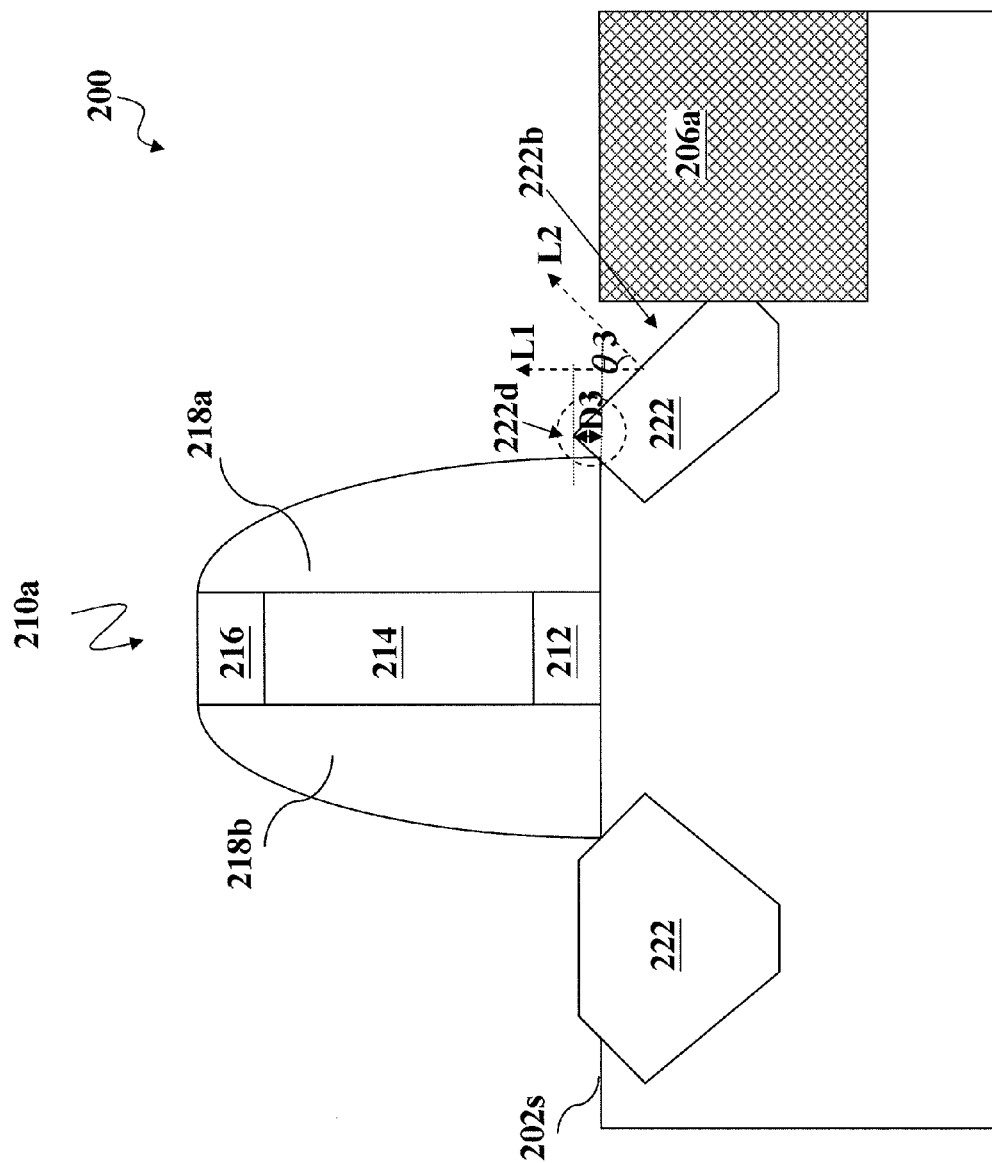


Fig. 5A

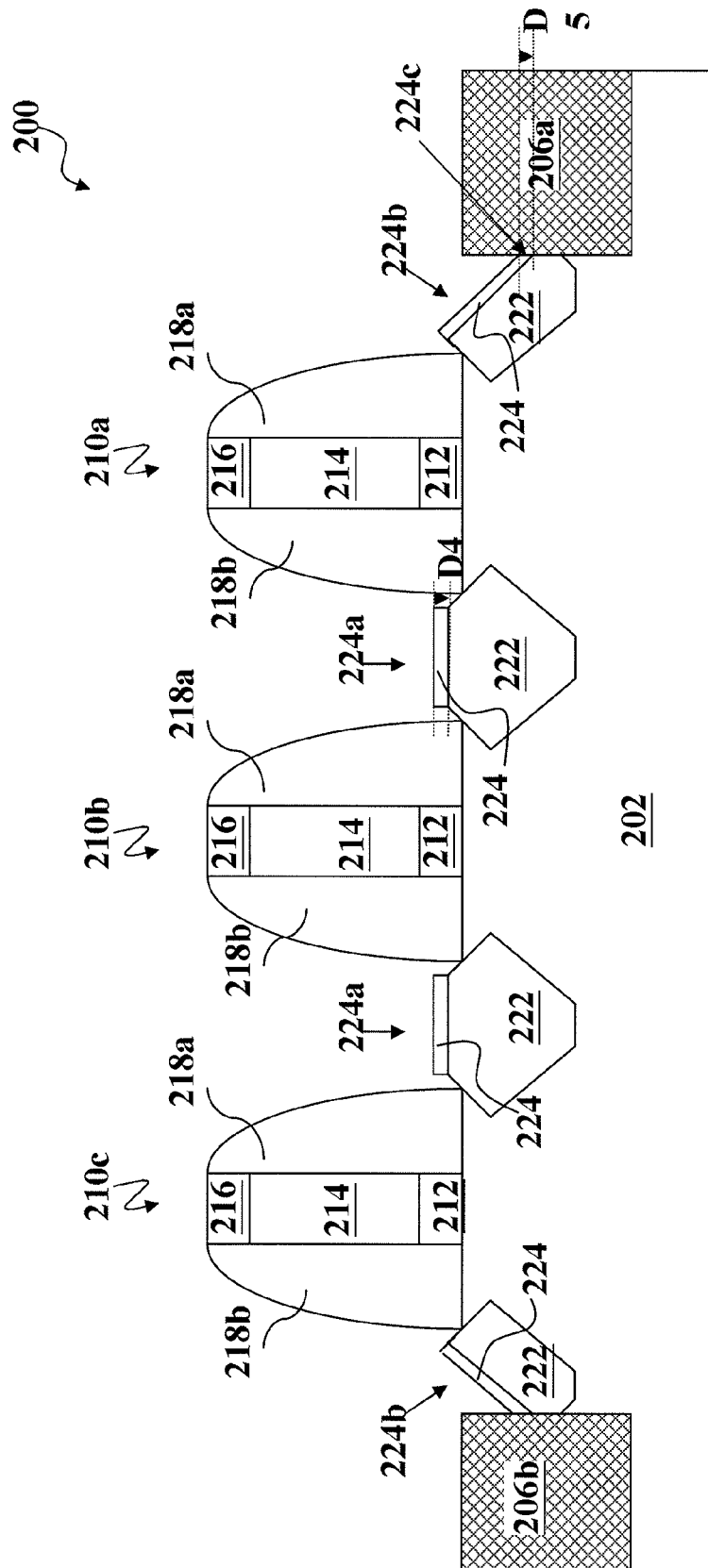


Fig. 6

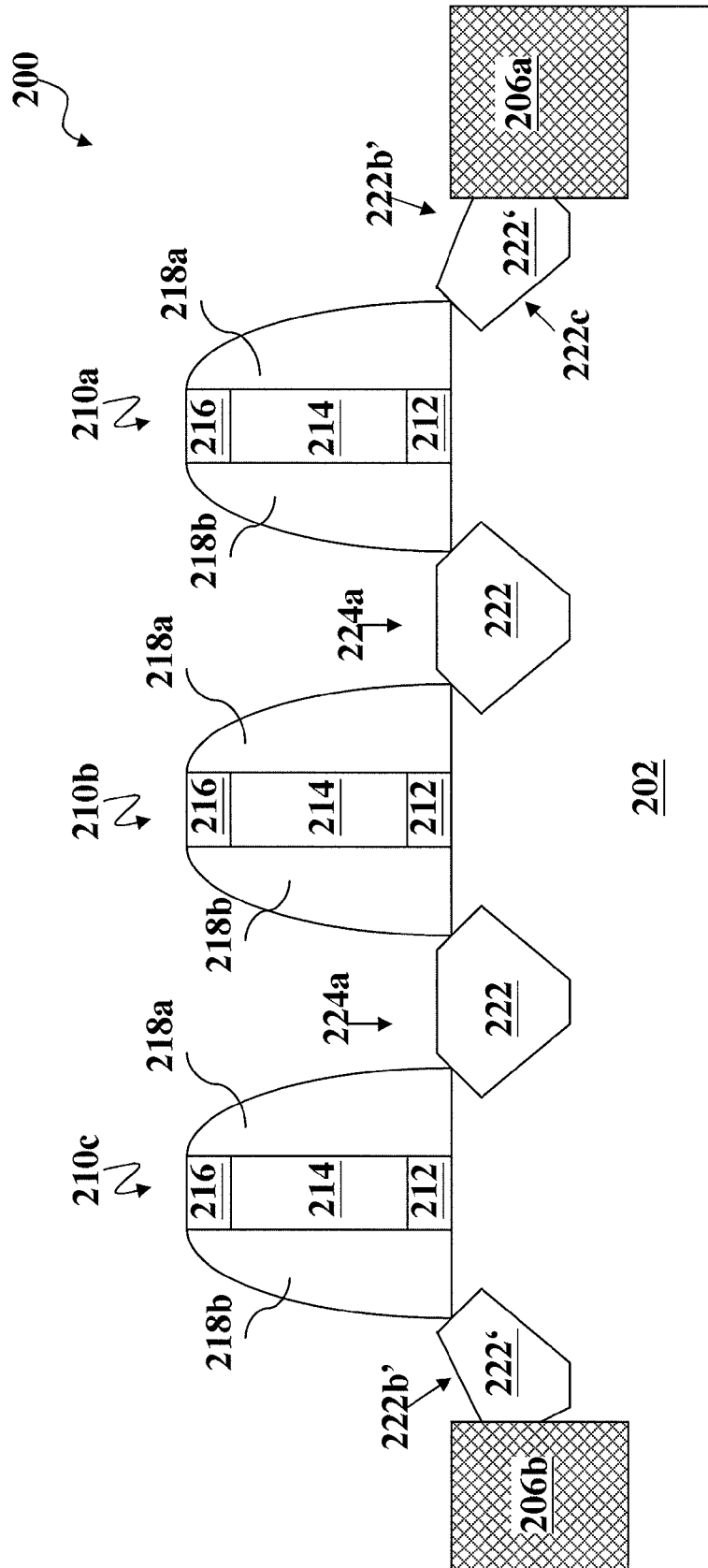


Fig. 7

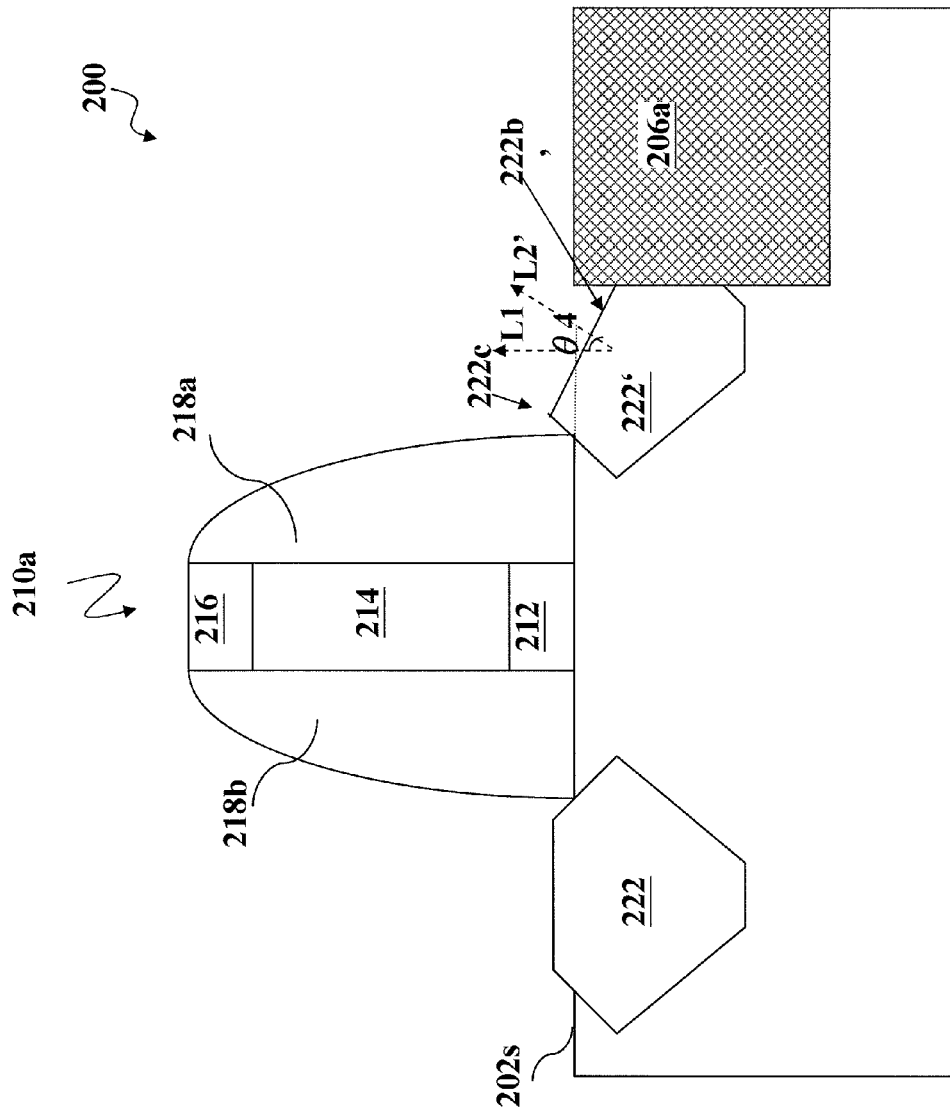


Fig. 7A

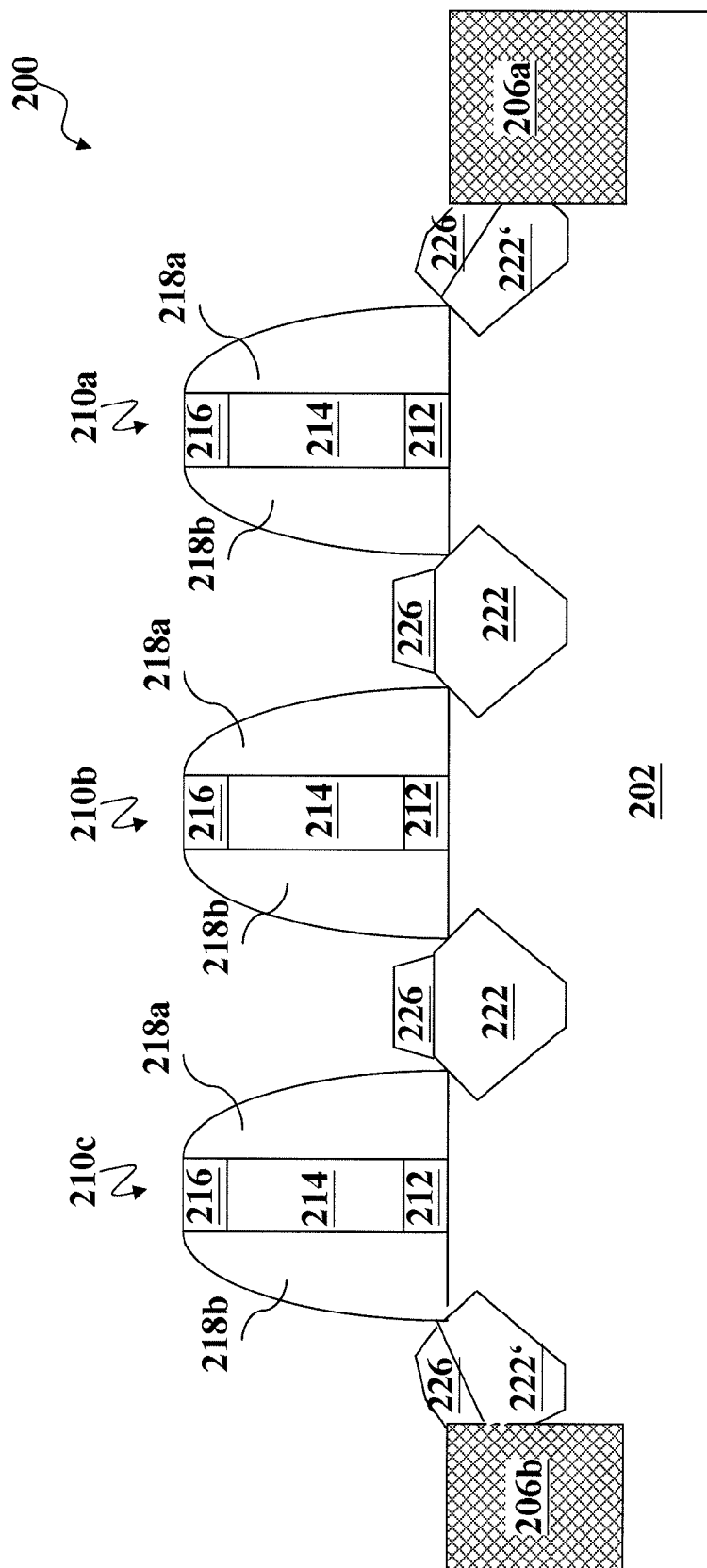


Fig. 8

1

SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF

PRIORITY CLAIM

The present application is a divisional of U.S. application Ser. No. 13/248,319, filed Sep. 29, 2011, the disclosure of which is incorporated herein by reference in its entirety.

FIELD

The disclosure relates to integrated circuit fabrication and, more particularly, to a semiconductor device with a strained structure.

BACKGROUND

When a semiconductor device, such as a metal-oxide-semiconductor field-effect transistor (MOSFET), is scaled down through various technology nodes, high-k gate dielectric layers and metal gate electrode layers are incorporated into the gate stack of the MOSFET to improve device performance with the decreased feature sizes. In addition, strained structures in source and drain (S/D) recess cavities of the MOSFET utilizing selectively grown silicon germanium (SiGe) may be used to enhance carrier mobility.

However, there are challenges to implement such features and processes in complementary metal-oxide-semiconductor (CMOS) fabrication. As the gate length and spacing between devices decrease, these problems are exacerbated. For example, it is difficult to achieve enhanced carrier mobility for a semiconductor device, because strained materials cannot deliver a given amount of strain into the channel region of the semiconductor device, thereby increasing the likelihood of device instability and/or device failure.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the relative dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 is a flowchart illustrating a method for fabricating a semiconductor device comprising a strained structure according to various aspects of the present disclosure; and

FIGS. 2-8 show schematic cross-sectional views of a strained structure of a semiconductor device at various stages of fabrication according to various aspects of the present disclosure.

DESCRIPTION

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct

2

contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

FIG. 1 is a flowchart illustrating a method 100 for fabricating a semiconductor device 200 according to various aspects of the present disclosure. FIGS. 2-8 show schematic cross-sectional views of a semiconductor device 200 at various stages of fabrication according to an embodiment of the method 100 of FIG. 1. The semiconductor device 200 may be included in a microprocessor, memory cell, and/or other integrated circuit (IC). It is noted that the method of FIG. 1 does not produce a completed semiconductor device 200. A completed semiconductor device 200 may be fabricated using complementary metal-oxide-semiconductor (CMOS) technology processing. Accordingly, it is understood that additional processes may be provided before, during, and after the method 100 of FIG. 1, and that some other processes may only be briefly described herein. Also, FIGS. 1 through 8 are simplified for a better understanding of the present disclosure. For example, although the figures illustrate the semiconductor device 200, it is understood the IC may comprise a number of other devices comprising resistors, capacitors, inductors, fuses, etc.

Referring to FIGS. 1 and 2, the method 100 begins at step 102 wherein a substrate 202 comprising a surface 202s is provided. In one embodiment, the substrate 202 comprises a crystalline silicon substrate (e.g., wafer). In the present embodiment, the substrate 202 is referred to as a (100) substrate having the surface 202s formed of the (100) crystal plane. In an alternative embodiment, the substrate 202 may include a silicon-on-insulator (SOI) structure.

The substrate 202 may further comprise active regions 204. The active regions 204 may include various doping configurations depending on design requirements. In some embodiments, the active regions 204 may be doped with p-type or n-type dopants. For example, the active regions 204 may be doped with p-type dopants, using a chemical such as boron or BF₂ to perform the doping; n-type dopants, using a chemical such as phosphorus or arsenic to perform the doping; and/or combinations thereof. The active regions 204 may act as regions configured for a N-type metal-oxide-semiconductor transistor device (referred to as an NMOS) and regions configured for a P-type metal-oxide-semiconductor transistor device (referred to as a PMOS).

In some embodiments, isolation structures 206a and 206b are formed in the substrate 202 to isolate the various active regions 204. The isolation structures 206a and 206b, for example, are formed using isolation technology, such as local oxidation of silicon (LOCOS) or shallow trench isolation (STI), to define and electrically isolate the various active regions 204. In the present embodiment, the isolation structures 206a and 206b include a STI. The isolation structures 206a and 206b may comprise silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), a low-K dielectric material, other suitable materials, and/or combinations thereof. The isolation structures 206a and 206b, and in the present embodiment, the STI, may be formed by any suitable process. As one example, the formation of the STI may include patterning the semiconductor substrate 202 by a photolithography process, etching a trench in the substrate 202 (for example, by using a dry etching, wet etching, and/or plasma etching process), and filling the trench (for example, by using a chemical vapor deposition process) with a dielectric material. In some embodiments, the filled trench

may have a multi-layer structure such as a thermal oxide liner layer filled with silicon nitride or silicon oxide.

Still referring to FIG. 2, in at least one embodiment, gate stacks **210a**, **210b**, and **210c** are formed over the surface **202s** of the substrate **202**. In some embodiments, the gate stacks **210a**, **210b**, and **210c** are formed by sequentially depositing and patterning a gate dielectric layer **212**, a gate electrode layer **214**, and a hard mask layer **216** on the substrate **202**.

The gate dielectric layer **212**, in one example, is a thin film comprising silicon oxide, silicon nitride, silicon oxynitride, high-k dielectrics, other suitable dielectric materials, or combinations thereof. High-k dielectrics comprise metal oxides. Examples of metal oxides used for high-k dielectrics include oxides of Li, Be, Mg, Ca, Sr, Sc, Y, Zr, Hf, Al, La, Ce, Pr, Nd, Sm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, Lu and mixtures thereof. In the present embodiment, the gate dielectric layer **212** is a high-k dielectric layer with a thickness in the range of about 10 angstroms to about 30 angstroms. The gate dielectric layer **212** may be formed using a suitable process such as atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), thermal oxidation, UV-ozone oxidation, or combinations thereof. The gate dielectric layer **212** may further comprise an interfacial layer (not shown) to reduce damage between the gate dielectric layer **212** and substrate **202**. The interfacial layer may comprise silicon oxide.

The gate electrode layer **214** is then formed on the gate dielectric layer **212**. In some embodiments, the gate electrode layer **214** may comprise a single layer or multilayer structure. In the present embodiment, the gate electrode layer **214** may comprise polysilicon. Further, the gate electrode layer **214** may be doped polysilicon with the same or different doping species. In one embodiment, the gate electrode layer **214** has a thickness in the range of about 30 nm to about 60 nm. The gate electrode layer **214** may be formed using a process such as low-pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), other suitable processes, or combinations thereof.

Next, the hard mask layer **216** is formed over the gate electrode layer **214** and a patterned photo-sensitive layer (not shown) is formed on the hard mask layer **216**. The pattern of the photo-sensitive layer is transferred to the hard mask layer **216** and then transferred to the gate electrode layer **214** and gate dielectric layer **212** to form the gate stacks **210a**, **210b**, and **210c** over the surface **202s** of the substrate **202**. In some embodiments, the hard mask layer **216** comprises silicon oxide. Alternatively, the hard mask layer **216** may comprise silicon nitride, silicon oxynitride, and/or other suitable dielectric materials, and may be formed using a method such as CVD or PVD. The hard mask layer **216** has a thickness in the range from about 100 angstroms to about 800 angstroms. The photo-sensitive layer is stripped thereafter by a dry and/or wet stripping process.

Referring to FIGS. 1 and 3, the method **100** proceeds to step **104** wherein gate spacers **218** are formed overlying opposite sidewalls of the gate stacks **210a**, **210b**, and **210c**. In the present embodiment, the gate spacers **218** adjoin sidewalls of the gate stacks **210a**, **210b**. In some embodiments, the gate spacers **218** may include a single-layer or a multiple-layer structure. In the present embodiment, a blanket layer of spacer material (not shown) is formed over the gate stacks **210a**, **210b**, and **210c** by a deposition process including CVD, PVD, ALD, or other suitable techniques. In some embodiments, the spacer material comprises silicon oxide, silicon nitride, silicon oxynitride, other suitable material, or combinations thereof. In some embodiments, the spacer material has a thickness ranging from about 5 nm to about 15 nm.

Then, an anisotropic etching is performed on the spacer material to form the gate spacers **218**.

Referring to FIGS. 1 and 4, the method **100** continues with step **106** in which the substrate **202** is recessed to form recess cavities **220**, **230**, **240**, and **250** in the substrate **202**. In some embodiments, the recess cavities **220**, **230**, **240**, and **250** are source and drain (S/D) recess cavities. In the structure of FIG. 4, the recess cavities **220** and **250** are formed between the gate stack **210a**/the isolation structure **206a** and the gate stack **210c**/the isolation structure **206b**, respectively. The recess cavities **230** and **240** are formed between the gate stacks **210a**/**210b** and **210b**/**210c**, respectively.

In the present embodiment, the processes for forming the recess cavities **220**, **230**, **240**, and **250** are started using an isotropic dry etching process, followed by an anisotropic wet or dry etching process. In some embodiments, the isotropic dry etching process is performed using the gate spacers **218** and isolation structures **206a** and **206b** as hard masks to recess the surface **202s** of the substrate **202** that is unprotected by the gate spacers **218** or the isolation structures **206a** and **206b** to form initial recess cavities (not shown) in the substrate **202**. In an embodiment, the isotropic dry etching process may be performed under a pressure of about 1 mTorr to about 1000 mTorr, a power of about 50 W to about 1000 W, a bias voltage of about 20 V to about 500 V, at a temperature of about 40° C. to about 60° C., using HBr and/or Cl₂ as etch gases. Also, in the embodiments provided, the bias voltage used in the isotropic dry etching process may be tuned to allow better control of an etching direction to achieve desired profiles for the S/D recess regions.

In some embodiments, a wet etching process is then provided to enlarge the initial recess cavities to form the recess cavities **220**, **230**, **240**, and **250**. In some embodiments, the wet etching process is performed using a chemical comprising hydration tetramethyl ammonium (TMAH), or the like. As a result of such etching processes, there may be formed a plurality of facets in each recess cavities **220**, **230**, **240**, and **250**. It should be noted that periphery environment with or without an etch stop can influence resultant features of the S/D recess cavities **220**, **230**, **240**, and **250**. During the wet etching process, the isolation structure **206a** may function as an etch stop for defining the recess cavity **220** between the gate stack **210a** and isolation structure **206a**. In some embodiments, the recess cavity **220** between the gate stack **210a** and isolation structure **206a** has respective sidewall surfaces defined by a bottom facet **220c**, an upper sidewall facet **220a**, lower sidewall facets **220b** and **220d**, and an upper portion of the sidewall of the isolation structure **206a**. Thereby, the facet **220a** and facet **220b** thus formed intersect each other and together define a wedge **220w** in the recess cavity **220**, such that the wedge-shaped recess cavity **220** extends into the substrate **202** in the region right underneath the spacer **218** toward the channel region. In some embodiments, the recess cavity **230** between the adjacent gate stacks **210a** and **210b** without an etch stop have respective sidewall surfaces each defined by a bottom facet **230c**, upper sidewall facets **230a** and **230e**, and lower sidewall facets **230b** and **230d**. Thereby, the facet **230d** and facet **230e** thus formed intersect each other and together define a wedge **230w** in the recess cavity **230**, such that the wedge-shaped recess cavity **230** extends into the substrate **202** in the region right underneath the spacer **218** toward the channel region.

In the illustrated example, the bottom facets **220c**, **230c** are formed of (100) crystal plane parallel to the crystal plane of the surface **202s** of the substrate **202**. In the illustrated example, the upper sidewall facets **220a**, **230a**, and **230e** and the lower sidewall facets **220b**, **220d**, **230b**, and **230d** are

5

formed of (111) crystal plane, and the upper sidewall facets **220a** and **230a** form an angle θ_1 to the bottom facets **220c** and **230c**. Further, the lower sidewall facets **220b** and **230b** form a smaller angle θ_2 than the angle θ_1 with respect to the bottom facets **220c** and **230c**. In the structure of FIG. 4, the angle θ_1 takes the range of about 90 degrees to about 150 degrees, while the angle θ_2 takes the range of about 40 degrees to about 60 degrees. In the present embodiment, the angles θ_1 and θ_2 take the values of 146 degrees and 56 degrees respectively in the case the facets **220a**, **230a**, **220b**, and **230b** are formed by the (111) crystal plane of the substrate **202**. However, it should be noted that the structure of FIG. 4 is not limited to the case in which the facets **220a**, **230a**, **220b**, and **230b** are formed by the (111) crystal plane.

Further, the bottom facet **220c** is formed at a depth D_1 as measured from the surface **202s** of the substrate **202**, while the upper facet **220a** is formed down to a depth D_2 . In the structure of FIG. 4, the depth D_1 is in the range of about 20 nm to about 70 nm, while the depth D_2 is in the range of about 5 nm to about 60 nm. By optimizing the depth D_2 and a distance between the mutually opposing wedges **220w**, **230w**, it becomes possible to confine the uniaxial compressive stress of a strained material **222** (shown in FIG. 5) effectively to the channel region, thereby enhancing the device performance.

The process steps up to this point have provided the substrate **202** having the recess cavities **220**, **230**, **240**, and **250** adjacent to the gate stacks **210a**, **210b**, and **210c**. Referring to FIGS. 1 and 5, the method **100** continues with step **108** in which a strained material **222** is grown in the recess cavities **220**, **230**, **240**, and **250** of the substrate **202** using a process including selective epitaxy growth (SEG), cyclic deposition and etching (CDE), chemical vapor deposition (CVD) techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy (MBE), other suitable epi processes, or combinations thereof. In some embodiments, the strained material **222** has a lattice constant different from the substrate **202** to induce a strain or stress on the channel region of the semiconductor device **200**, and therefore enable carrier mobility of the device to enhance the device performance.

In the present embodiment, a pre-cleaning process is performed to clean the recess cavities **220**, **230**, **240**, and **250** using a chemical comprising hydrofluoric acid (HF) or other suitable solution. Then, gaseous and/or liquid precursors may be provided to interact with the composition of the substrate **202** to form the strained material **222**, such as silicon germanium (SiGe), to fill the recess cavities **220**, **230**, **240**, and **250**. In one embodiment, the process for forming the strained material **222** comprising SiGe is performed at a temperature of about 600° to 750° C. and under a pressure of about 10 Torr to about 80 Torr, using reaction gases comprising SiH_2Cl_2 , HCl, GeH_4 , B_2H_6 , H_2 , or combinations thereof. In some embodiments, a ratio of a mass flow rate of the SiH_2Cl_2 to a mass flow rate of the HCl is in the range of about 0.45 to 0.55. In one embodiment, the strained material **222** is therefore grown from the facets **230a**, **230b**, **230c**, **230d**, and **230e** to the center of the recess cavity **230** in the substrate **202**. In another embodiment, the strained material **222** is therefore grown from the facets **220a**, **220b**, **220c**, and **220d** to the center of the recess cavity **220** in the substrate **202**.

In some embodiments, the growth of the strained material **222** in the recess cavity **230** that is not adjacent to the isolation structure **206a** is mainly along the facet **230c** and therefore has an upper surface **222a** formed of (100) crystal plane. In the present embodiment, the growth of the strained material **222** in the recess cavity **220** that is adjacent to the isolation structure **206a** is limited by the isolation structure **206a**

6

because the isolation structure **206a** formed by dielectric with an amorphous structure fails to offer nucleation sites to grow an epitaxial material. In some embodiments, the growth of the strained material **222** in the recess cavity **220** tends to have an upper surface **222b** formed of (111) crystal plane with a stable surface energy. The strained material **222** in the recess cavity **220** has a lower sidewall surface **222c** formed over the lower sidewall facet **220b** and therefore is formed of (111) crystal plane. In some embodiments, the lower sidewall surface **222c** is parallel to the upper surface **222b**. It can be seen in FIG. 5 that the strained material **222** adjacent to the isolation structure **206a** occupies a small portion of the recess cavity **220**.

In FIG. 5A, the semiconductor device **200** is enlarged for better understanding of the profile of the strained material **222** in the recess cavity **220**. In the present embodiment, the strained material **222** in the recess cavity **220** has a corner **222d** adjacent to the edge of the gate stack **210a** and having a tip higher than the surface **202s** of the substrate **202**. The corner **222d** has a height D_3 measured from the surface **202s** to the tip of the corner **222d**. In some embodiments, the height D_3 ranges between about 1 nm and about 10 nm. As shown in FIG. 5A, there are a normal line **L1** perpendicular to the surface **202s** of the substrate **202**, a normal line **L2** perpendicular to the upper surface **222b** of the strained material **222** in the recess cavity **220**, and an angle θ_3 between the normal line **L1** and the normal line **L2**. As mentioned above, the substrate **202**, for example, is a (100) substrate having the surface **202s** formed of the (100) crystal plane, and the upper surface **222b** is formed of (111) crystal plane. Therefore, in the present embodiment, the angle θ_3 is about 54 degrees.

Referring to FIGS. 1 and 6, the method **100** continues with step **110** in which a cap layer **224** is formed over the strained material **222**. The cap layer **224** may function as a protection layer to prevent the underlying strained material **222** from being over-etched in a subsequent etching process. In the present embodiment, the cap layer **224** is formed by an epi growth process. The cap layer **224** over the strained material **222** in the recess cavity **230**, which is not adjacent to the isolation structure **206a**, has a thickness D_4 . In some embodiments, the thickness D_4 ranges between about 1 nm and about 5 nm. The cap layer **224** over the strained material **222** in the recess cavity **220** adjacent to the isolation structure **206a** has a sidewall **224c** contacting the isolation structure **206a** with a thickness D_5 . In some embodiments, a ratio of the thickness D_4 over the thickness D_5 ranges between about 1 and about 3. In some embodiments, the cap layer **224** over the strained material **222** in the recess cavities **230** may grow along the crystal orientation of the upper surface **222a** and has an upper surface **224a** formed of (100) crystal plane. In some embodiments, the cap layer **224** over the strained material **222** in the recess cavities **220** may grow along the crystal direction of the upper surface **222b** and has an upper surface **224b** formed of (111) crystal plane.

In some embodiments, the cap layer **224** comprises a material different from the strained material **222**. In some embodiments, the cap layer **224** is a silicon-containing layer. In the present embodiment, the cap layer **224** is silicon. In some embodiments, the cap layer **224** is formed by a process including selective epitaxy growth (SEG), cyclic deposition and etching (CDE), chemical vapor deposition (CVD) techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy (MBE), other suitable epi processes, or combinations thereof. In the present embodiment, the cap layer **224** is formed by a process that is the same as the process for forming the strained material **222**. In some embodiments, the cap layer **224** is continuously formed after forming the strained material **222**

by changing the process conditions to be performed at a temperature of about 700° C. to about 800° C., under a pressure of about 10 Torr to about 50 Torr, and using a silicon-containing gas (e.g., SiH₂Cl₂) as reaction gas. In an alternative embodiment, B₂H₆ and/or H₂ are introduced with the silicon-containing gas for forming the cap layer 224.

Referring to FIGS. 1 and 7, the method 100 continues with step 112 in which an etching process is provided to the semiconductor device 200. In some embodiments, the etching process is in-situ performed in the equipment for forming the cap layer 224 (e.g., CVD equipment), whereby there is not vacuum break between the step for forming the cap layer 224 and the step for performing the etching process. In alternative embodiments, the cap layer 224 is omitted and the etching process is in-situ performed in the equipment for forming the strained material 222. In the present embodiment, the etching process is performed by introducing an etching gas over the cap layer 224 and the strained material 222 without providing a power source or generating plasma. In an embodiment, the etching gas is a chlorine-containing gas, such as Cl₂ and/or HCl. In an alternative embodiment, the etching process is performed using the etching gas and a carrier gas, e.g., H₂ and/or N₂. In the present embodiment, the etching gas has a flow rate ranging between about 50 sccm and about 300 sccm, and the carrier gas has a flow rate ranging between about 3 slm and about 4 slm (standard liter per minute).

In some embodiments, the cap layer 224 is removed in the etching process to expose the underlying strained material 222. Next, in an embodiment, a treated strained material 222' is formed in the recess cavity 220 by redistributing at least a portion of the corner 222d of the strained material 222 to be located in the recess cavity 220. The redistribution may increase an amount of the strained material 222 in the recess cavity 220, therefore fabricate a large-volume strained structure to enhance carrier mobility and upgrade the device performance of the semiconductor device 200. In an alternative embodiment, the corner 222d above the surface 202s of the substrate 202 is redistributed to be completely located in the recess cavity 220, therefore all the treated strained material 222' is within the recess cavity 220. Meanwhile, there is not a redistribution process performed on the strained material 222 in the recess cavities 230, 240.

In one embodiment, the redistribution results due to reducing the high surface energy of the tip in corner 222d. In an alternative embodiment, the redistribution results due to a reflow process in the etching process. The original upper surface 222b of the strained material 222 in the recess cavity 220 is transformed into a treated upper surface 222b' after the etching process. In some embodiments, the treated upper surface 222b' has a transformed crystal plane deviated from the original (111) crystal plane, therefore, the lower sidewall surface 222c of the treated strained material 222' is not parallel to the treated upper surface 222b'. In the present embodiment, the treated upper surface 222b' has a (311) crystal plane. In FIG. 7A, the semiconductor device 200 is enlarged for better understanding of the profile of the treated strained material 222'. As shown in FIG. 7A, the normal line L1 is perpendicular to the surface 202s of the substrate 202, a normal line L2' is perpendicular to the treated upper surface 222b' of the treated strained material 222' in the recess cavity 220, and an angle θ_4 is between the normal line L1 and the normal line L2'. In one embodiment, the angle θ_4 is less than the angle θ_3 . In another embodiment, the angle θ_4 is about 25-35 degrees.

Referring to FIGS. 1 and 8, the method 100 continues with step 114 in which contact features 226 are formed over the treated strained material 222' in the recess cavities 220, 250

and the strained material 222 in the recess cavities 230, 240. In the present embodiment, the contact features 226 are formed by a process that is the same as the process for forming the strained material 222 or the cap layer 224. The contact features 226 may provide a low contact resistance between the cap layer 224 and a silicide structure formed subsequently. In at least one embodiment, the contact features 226 have a thickness ranging from about 150 Angstroms to about 200 Angstroms. In some embodiments, the contact features 226 comprise a material that is the same as the material of cap layer 224. In alternative embodiments, the contact features 226 comprise a material that is the same as the material of strain material 222.

It is understood that the semiconductor device 200 may undergo further CMOS processes to form various features such as contacts/vias, interconnect metal layers, dielectric layers, passivation layers, etc. In some embodiment, the gate stacks 210a, 210b, and 210c may be dummy gate stacks. Thus, the CMOS processes further comprise a "gate last" process to replace the polysilicon gate electrode with a metal gate electrode to improve device performance. In one embodiment, the metal gate electrode may include a metal such as Al, Cu, W, Ti, Ta, TiN, TiAl, TiAlN, TaN, NiSi, CoSi, other suitable conductive materials, or combinations thereof. It has been observed that the modified strained structure provides a given amount of strain into channel region of a semiconductor device, thereby enhancing the device performance.

The various embodiments of the present disclosure discussed above offer advantages over conventional methods, it being understood that no particular advantage is required for all embodiments, and that different embodiments may offer different advantages. One of the advantages is that the lower portion of the strained material in the S/D recess cavity adjacent to the isolation structure may be increased to enhance carrier mobility and upgrade the device performance. Another advantage is that the likelihood of device instability and/or device failure that results due to forming a subsequent silicide over the lower portion of the strained material may be prevented.

In one embodiment, a method for fabricating a semiconductor device includes forming an isolation feature in a substrate, forming a gate stack over the substrate, forming a source/drain (S/D) recess cavity in the substrate, where the S/D recess cavity is positioned between the gate stack and the isolation feature. The method further includes forming an epitaxial (epi) material in the S/D recess cavity, where the epi material has an upper surface which including a first crystal plane. Additionally, the method includes performing a redistribution process to the epi material in the S/D recess cavity using a chlorine-containing gas, where the first crystal plane is transformed to a second crystal plane after the redistribution.

In another embodiment, a semiconductor device includes a gate stack over a substrate, an isolation feature in the substrate, a recess cavity in the substrate between the gate stack and the isolation feature. Additionally, the semiconductor device includes an epitaxial (epi) material in the recess cavity, where the epi material has a first crystal plane at a bottom surface of the recess cavity. Furthermore, the semiconductor device includes a second crystal plane at a top surface of the recess cavity, where the first crystal plane is different from the second crystal plane. The semiconductor device further includes a contact feature over the epi material.

In still another embodiment, a semiconductor device includes a gate stack over a substrate, an isolation feature in the substrate, a recess cavity in the substrate between the gate stack and the isolation feature. Additionally, the semiconduc-

tor device includes an epitaxial (epi) material in the recess cavity, where the epi material includes a (111) crystal plane and a (311) crystal plane.

While the disclosure has described by way of example and in terms of the preferred embodiments, it is to be understood that the disclosure is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A semiconductor device comprising:
a gate stack over a substrate;
an isolation feature in the substrate;
a recess cavity in the substrate between the gate stack and the isolation feature;
an epitaxial (epi) material in the recess cavity, the epi material has a first crystal plane at a side surface connecting to a bottom surface and a second crystal plane at an upper surface contacting the isolation feature, the bottom surface being substantially parallel to a top surface of the substrate, wherein the first crystal plane is different from the second crystal plane; and
a contact feature over the epi material, wherein the contact feature extends along a sidewall of the isolation feature.
2. The semiconductor device of claim 1, wherein the substrate comprises a silicon-on-insulator structure.
3. The semiconductor device of claim 1, wherein the isolation feature comprises at least one of silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), or a low-K dielectric material.
4. The semiconductor device of claim 1, wherein the gate stack comprises a gate electrode layer.
5. The semiconductor device of claim 4, wherein the gate electrode layer has a thickness ranging from 30 nanometers (nm) to 60 nm.
6. The semiconductor device of claim 1 further comprising a hard mask layer over the gate stack.
7. The semiconductor device of claim 6, wherein the hard mask layer has a thickness ranging from 100 Angstroms (Å) to 800 Å.
8. The semiconductor device of claim 1 further comprising gate spacers on opposite sidewalls of the gate stacks.
9. The semiconductor device of claim 8, wherein the gate spacers have a thickness ranging from 5 nm to 15 nm.

10. A semiconductor device comprising:
a gate stack over a substrate;
an isolation feature in the substrate;
a recess cavity in the substrate between the gate stack and the isolation feature;
an epitaxial (epi) material in the recess cavity, wherein the epi material has a first crystal plane at a side surface directly connected to a bottom surface of the recess cavity and a second crystal plane at an upper surface adjacent to the isolation feature, and the epi material extends along a portion of a sidewall of the isolation feature; and
a contact feature over the epi material.
11. The semiconductor device of claim 10, wherein the contact feature contacts the sidewall of the isolation feature.
12. The semiconductor device of claim 11, wherein the contact feature has a thickness ranging from 1 nm to 5 nm.
13. The semiconductor device of claim 11, wherein the contact feature comprises a material different from the epi material.
14. The semiconductor device of claim 10, wherein a vertical distance from an uppermost region of the substrate to a lowest region of the recess cavity ranges from 20 nm to 70 nm.
15. The semiconductor device of claim 10, wherein the epi material has a (311) crystal plane over the first crystal plane.
16. A semiconductor device comprising:
a gate stack over a substrate;
an isolation feature in the substrate;
a recess cavity in the substrate between the gate stack and the isolation feature;
an epitaxial (epi) material in the recess cavity, wherein the epi material has a first crystal plane at a side surface directly connected to a bottom surface of the recess cavity and a second crystal plane at an upper surface connected to the isolation feature of the recess cavity, and the epi material includes a surface substantially parallel to a sidewall of the isolation feature; and
a contact feature over the epi material.
17. The semiconductor device of claim 16, wherein the first crystal plane is a (111) crystal plane.
18. The semiconductor device of claim 16, wherein the contact feature contacts a sidewall of the isolation feature.
19. The semiconductor device of claim 18, wherein the contact feature comprises a material different from the epi material.
20. The semiconductor structure of claim 16, wherein the epi material further comprises a (100) crystal plane.

* * * * *